1/4 B.Tech SECOND SEMESTER

IT2L2 DIGITAL LOGIC DESIGN LAB Credits: 2

Lecture: -- Internal assessment: 25 marks
Lab : 3 periods/week Semester end examination: 50 marks

Objectives:

- Verification of Boolean algebra and truth tables.
- Verification of half-adder and full-adder and its truth tables.
- Verification of converters Binary-decimal, binary-Hexadecimal, Binary-Gray.
- Implementation and verification of Decoder/ De-multiplexer and Encoder using logic gates.
- Implementation of 8*1 multiplexer using logic gates.
- Verification of state tables of RS,JK,T and D flip-flops using NAND & NOR gates.
- Verification of Basic Shift Registers.

Outcomes:

The student will be able to

- Get familiar with numbering systems and converting one number system to other.
- Get familiar with half-adder and full-adder logic circuits.
- Get familiar with Decoder, Encoder, Multiplexer and De-multiplexer circuits.
- Get familiar with Flip-Flops and its Circuitry.
- Get familiar with basic shift registers and its circuitry.
- Develop and Build simple circuits.

Exercise 1

Boolean algebra Theorems and logical guides, verification of truth tables

Exercise 2

Realization of Boolean expressions Using (i) AND – OR-NOT Gates (ii) NAND Gates (iii) NOR Gates

Exercise 3

Adders / Sub tractors Half Adder, Full Adder, 1‘s and 2’s complement addition

Exercise 4

Code Converters Decimal –to-Binary, Binary – to – Decimal, Decimal – to- Hexa Decimal.

Exercise 5

Code Converters BCD- to –Decimal, Binary – to- gray, gray- to -Binary

Exercise 6
Multiplexers/ Data Selector 2- input and 8- input, De-multiplexers, Logic Function Generator

Exercise 7
Decoders and Encoders.

Exercise 8
BCD adders and Comparators

Exercise 9
Latches Flip – Flops RS, JK,T,D, Master –Slave FF, Edge – Triggered Flip – Flops.

Exercise 10
Counters Binary Counter, Ripple Counter, Up/Down Counter, BCD Counter.

Exercise 11
Registers Basic Shift Register (SR), SI/SO SR, SI/PO SR, PI/SO SR, PI/PO SR.

Exercise 12
Ring /Johnson Counter, Sequence Generator, Parity Generators/ Checkers.

REFERENCE BOOK:

1.Digital Logic and Computer Design By M.Moris Mano 4th Edition